

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES



Ex parte YANNICK VINCENT

Appeal No. 2005-0859
Application No. 10/015,965

ON BRIEF

Before BARRETT, OWENS, and RUGGIERO, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from a rejection of claims 1-9, which are all of the pending claims.

THE INVENTION

The appellants claim a data processing system and terminal comprising a hardware circuit for inverting an order of bits of a word as a function of a value of a convention signal. Claims 1 and 9 are illustrative:

1. A data-processing system, comprising:
a microprocessor [PRC];
a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].

9. A data-processing system, comprising:
a hardware circuit [HARD];
a communication device [COM] for communicating a contention [sic, convention] signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]; and
wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the words as a function of a value of the convention signal.

THE REFERENCES

Muwafi et al. (Muwafi)	5,978,822	Nov. 2, 1999
Van Rensburg et al. (Van Rensburg)	US 2003/0004891 A1 (PCT filed Jan. 29, 2001)	Jan. 2, 2003
Chiang	6,574,776	Jun. 3, 2003 (filed Apr. 9, 1999)

THE REJECTIONS

The claims stand rejected as follows: claims 1, 3, 5, 7 and 9 under 35 U.S.C. § 102(b) as anticipated by Chiang; claims 2 and 6 under 35 U.S.C. § 103 as obvious over Chiang in view of Van Rensburg; and claims 4 and 8 under 35 U.S.C. § 103 as obvious over Chiang in view of Muwafi.

OPINION

We reverse the aforementioned rejections.

Independent claims 1 and 5 require a hardware circuit that allows an inversion of an order of bits of a word as a function of a value of a convention signal during a transfer of a word between an electronic module and a microprocessor. Independent

claim 9 requires a hardware circuit that includes means for implementing one of a direct convention and an indirect convention of an order of bits of a word as a function of a value of a convention signal.

The examiner argues that Chiang's data communication between memory unit 11 and the processors (ECD processor 13 and ECC-P processor 15; figure 1) is a "conventional signal" (answer, pages 3-4). The appellant's claims 1, 5 and 9, however, do not recite a "conventional signal" but, rather, recite a "convention signal". The appellant's specification discloses a convention bit that is generated from either a direct convention signal or an indirect convention signal and has a value of 0 when the direct convention is used and 1 when the indirect convention is used (page 4, line 32 - page 5, line 7). The portion of Chiang relied upon by the examiner for a disclosure of a "conventional signal" (col. 1, line 66 - col. 2, line 26) does not disclose a convention signal. The portion of Chiang relied upon by the examiner for a disclosure of a hardware circuit that allows an inversion of an order of bits of a word as a function of a value of a convention signal during a transfer of a word between an electronic module and a microprocessor (figure 7; col. 6, line 59 - col. 7, line 48) does not disclose either a convention signal or allowing an inversion of an order of bits of a word as a function of a value of a convention signal during a transfer of a

word between an electronic module and a microprocessor. The examiner does not cite any portion of Chiang for a disclosure of the claim 9 hardware circuit that includes means for implementing one of a direct convention and an indirect convention of an order of bits of a word as a function of a value of a convention signal.

We therefore find that the examiner has not carried the burden of establishing a *prima facie* case of anticipation of the inventions claimed in the appellant's independent claims 1, 5 and 9 or dependent claims 3 and 7 which depend, respectively, from claims 1 and 5.


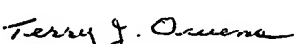
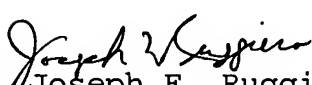
As for the claims rejected under 35 U.S.C. § 103, the examiner does not rely upon Chiang, alone or in combination with Van Rensburg or Muwafi, for any disclosure that would have fairly suggested, to one of ordinary skill in the art, the above-discussed claim features that are not disclosed by Chiang.

Accordingly, we conclude that the examiner has not established a *prima facie* case of obviousness of the inventions claimed in the appellant's claims 2, 4, 6 and 8.

DECISION

The rejections of claims 1, 3, 5, 7 and 9 under 35 U.S.C. § 102(b) over Chiang, claims 2 and 6 under 35 U.S.C. § 103 over Chiang in view of Van Rensburg, and claims 4 and 8 under 35 U.S.C. § 103 over Chiang in view of Muwafi, are reversed.

REVERSED

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Lee E. Barrett)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
Terry J. Owens)	
Administrative Patent Judge)	APPEALS AND
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)	INTERFERENCES
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Joseph F. Ruggiero)	
Administrative Patent Judge)	

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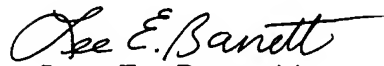
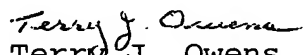
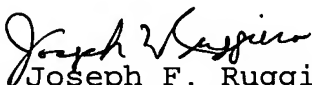
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